ALMA MATER STUDIORUM - UNIVERSITÀ DI BOLOGNA

ELECTRIC VEHICLE ENGINEERING - MUNER

COURSE:

AUTOMOTIVE POWER ELECTRONIC CIRCUITS DESIGN M

PFC BOOST CONVERTER

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Student :

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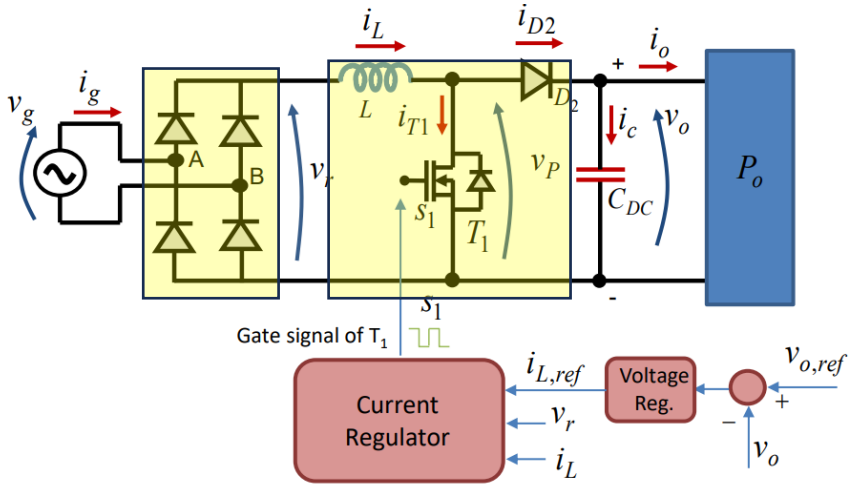
Introduction

A power factor corrector is a switching mode converter that allow to have a control bandwidth for the output voltage control that can reach hundreds of Hertz that bring the possibility to have compact filters and It can actively suppress low frequency harmonics of the line current, leading to a very low THD values.

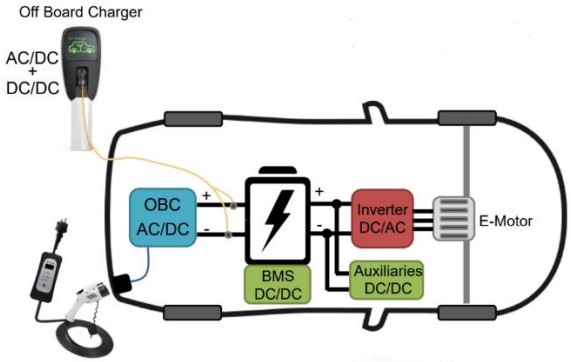
The PFC boost converter is a topology of AC/DC converter that are usually employed in the front end of an on board battery charge for an electric vehicle. It is a single phase unidirectional converter. It is composed of two main stage, the first one is a diode bridge rectifier and the second one is a boost type converter.



An ideal power factor corrector aim to emulate a resistor and the expected grid waveform will be sinusoidal with a THD =0 and the ripple of the output voltage is zero. The real configuration should try to achieve a result that is the closest as possible to the ideal one (or that satisfy the requested design constrain). By acting on the duty cycle of the boost cell is possible to tune the desired output voltage thanks to a control strategy that introduce a close control loop and also affect the input grid current.

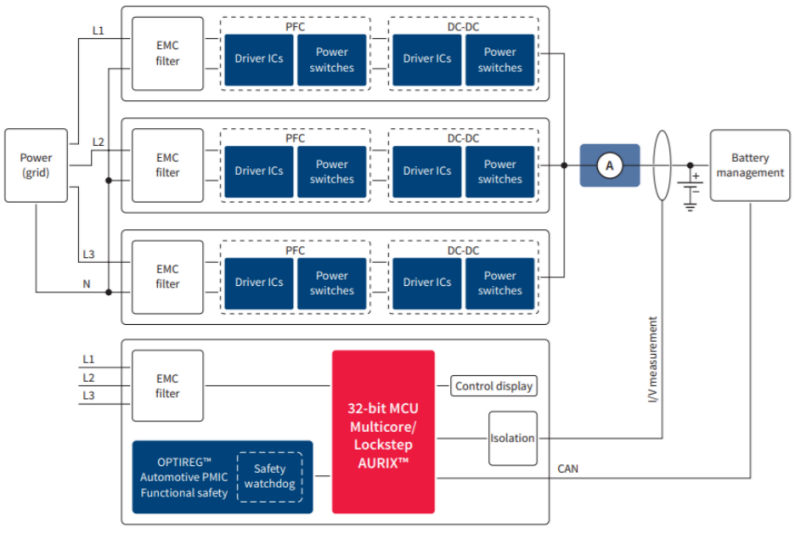
In this design process the stary parameters of the circuit and of the devices are taken into account but for the electrical system-level simulation on PLECS some of them are neglected in order to focus in a first time the attention on the dynamic and electrical behavior of this topology and find the degree of freedom before entering in the detail by considering also the dynamic behavior of the switch and so on. Also a thermal simulation was done in order to provide a physical demonstration of how the power losses are affecting the temperature of the single devices but also of the overall circuit.

The most common application is on the on board charger of battery electric vehicles where it provide to the battery a constant voltage by thanking the power from an grid (In this study case a monophase grid).



In order to provide to the vehicle user the possibility of charging is car also to an AC three phase grid, it is possible to see this configuration in parallel with other two to obtain a three phase PFC. This solution do not implies a three phase diode rectifier because of the line current harmonics cannot be fully controlled when two diodes of the bridge are conducing at the same time, that lead one of the three phase down to zero and to recover to this behavior are needed input filters to reduce the THD of the line current. This never happen in single phase topology since a low THD can be achieved automatically by the converter that by simply operating is able to actively suppress the low frequency harmonics of the line current.

	SAE J1772		IEC 61851	
	AC LEVEL 1	**AC LEVEL 2**	**MODES 1**	**MODES 2–3**
Maximum power	1.9 kW	19.2 kW	4 kW (13.3 kW)	8 kW (22 kW)
Input voltage	120 V, single phase	240 V, split phase	250 V, single phase (480 V, three phase)	250 V, single phase (480 V, three phase)
Maximum current	16 A	80 A	16 A	32 A
Communication	PLC	PLC	None	PLC
Region	United States, Japan, South Korea		Europe, Australia	
Related standards	• IEC 61851-22/23 • IEC 62196-2 • SAE J1772-2017		• IEC 61851-22/23 • IEC 62196-2	
Vehicle to device	Under development		Under development	
Plug type				
Example	 Blink level 2, wall mount: 208–240 V, single phase, 30 A, 7.2 kW		 Siemens VersiCharge: 230 V, three phase, 32/22 kW	



Requirements

Power stage of a Boost PFC Converter used as a front end of an On-Board Battery Charger of an electric vehicle with the following characteristics:

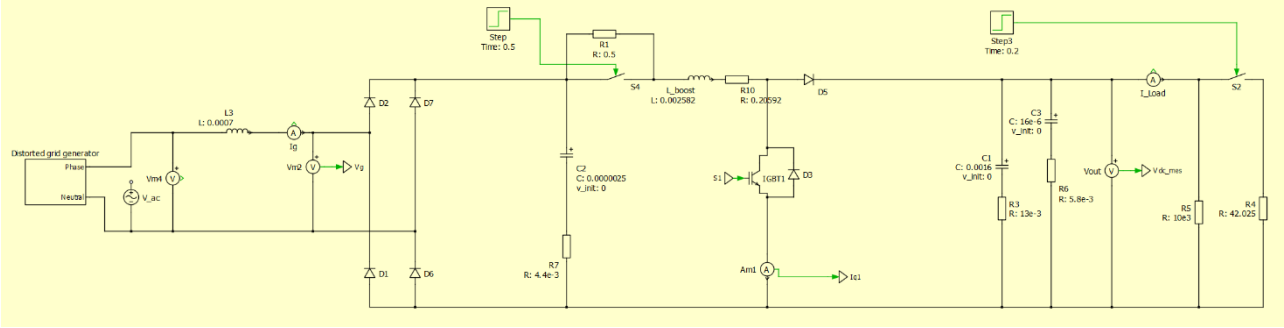
• Grid voltage 230 VRMS at 50 Hz (±10% tolerance on the magnitude of the voltage).

• Rated output voltage 410 V with a ripple lower than 5%

• Rated output power 4000 W • Switching frequency 16 kHz

• Forced air cooling, maximum ambient temperature 50°C.

Design description

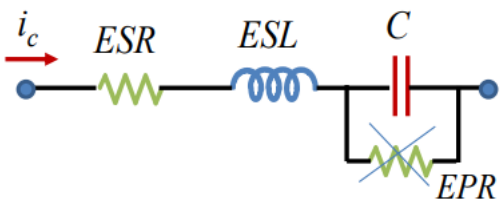


Design passive device

In order to provide a more realistic simulation on PLECS, the design of each component is needed. Staring from the passive component and then moving to the active ones, this design workflow is devoted to obtain all the result that characterize each devices, even some stray beavers are taken into consideration in order to be able in a second moment to validate the simulation even on simulation software like SPICE that take into consideration also detailed analysis of electrical stimulation.

Capacitors

A capacitor consists in two conductors separated by a layer of insulating material (the dielectric). The conducting surfaces can be plates, foil, solid shapes, or even wires. The separator can be air, vacuum, a metal oxide layer (as in electrolytic capacitors), a flat thin paper, or a plastic film.
During the electrical simulation, the behavior of the capacitor is reduced to a series of a capacitance and a resistance, in reality the full scheme of a capacitor is the following:



There are also present an inductive contribute in series with the two precedent, the inductive contribution is predominant when the system work in a region where the operating frequency is above the resonant one provide by this system. Moreover the resistance in parallel to the capacitance have very low impact in the power balance, but it is the main actor for the self-discharge, so if this effect is under investigation, this parameter should be included.

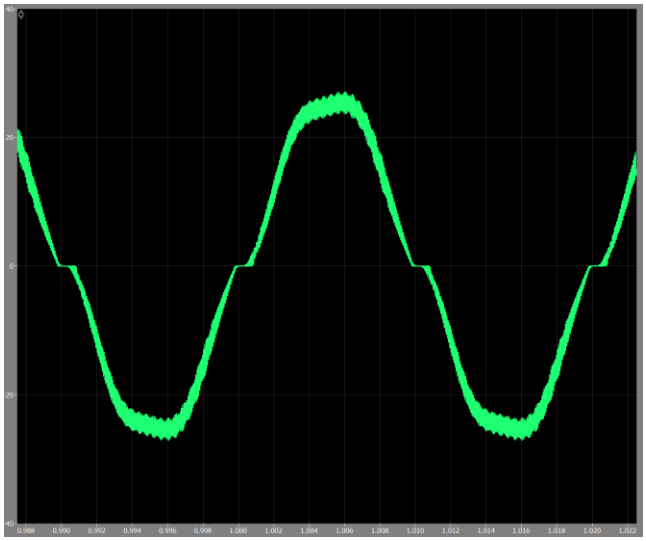
The capacitor present in this simulation are three: the input capacitor and the two output capacitor.

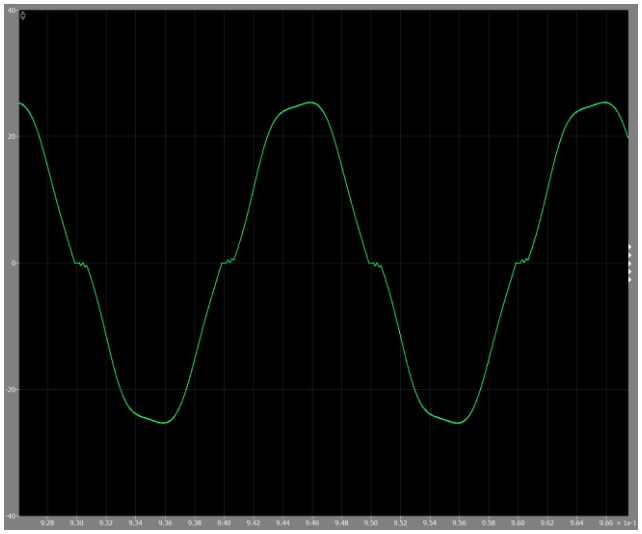
HF Input capacitance:

an input capacitance is needed after the diode bridge because since the control scheme that it is used in these simulation introduces a current ripple on the inductor current, it is a suggested to put on high frequency component that bypass the high frequency and let the grid current work by only containing low frequency component (the is effect is more evident in presence of control strategies like the critical current mode control that can lead to have an high ripple of the boost inductor current). Generally it is important to not exceed in the value of the capacitance in order to be far from the behavior of are bridge rectifier. So a film capacitor can be a good solution.

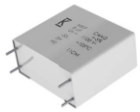
The equation to support these design are based on the assumption of trying to reach an ideal PF, so for sure this estimation can be improved in a deeper analysis. Now it is enough to consider the capacitance in relation of the ripple and also by the simulation this value ended up to be a good value for this project.

(0.27 μF an the right and 2.7 μF on the left)



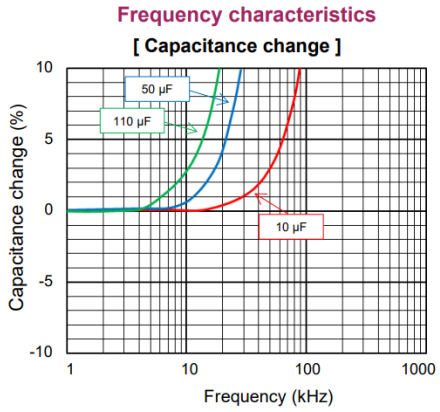


By looking to the catalogue provided by KENET is possible to obtain the values for the ESR and ESL (the EPL is neglected since it is a lower value in comparison with those three)

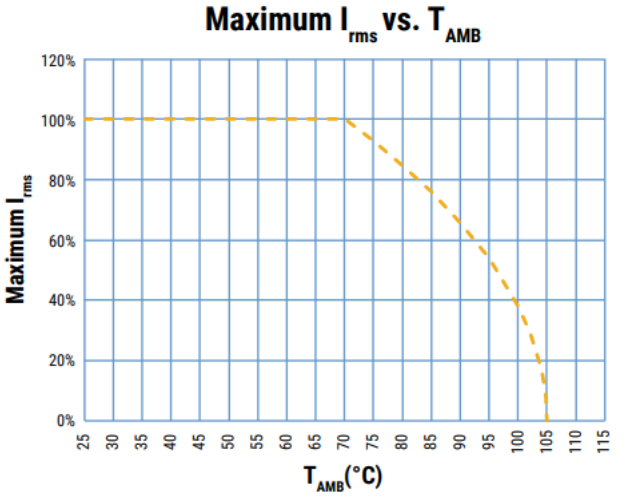


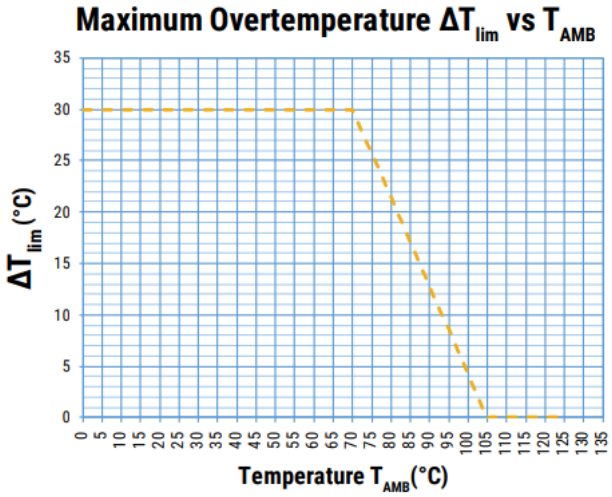
Cap Value (µF)	VDC	Dimensions (mm)					dV/dt	Ipkr	ESL	ESR 70°C at 10 kHz	Irms* 70°C at 10 kHz	Rth (HS/Amb)	Packaging Quantity	PART NUMBER
		T	H	L	S	S1	V/µs	Apk	nH	mΩ	Arms	(°C/W)		
V_{NDC} at 70°C = 800 VDC; V_{OP85} at 85°C = 700 VDC; V_{OP105} at 105°C = 550 VDC														
2.7	800	11	20	31.5	27.5	\	19	51	17	18.3	5.7	44	256	C4AQIBU4270A1WJ

This values like the ESR, ESL, maximum current… are evaluate by looking to the table that compare the these values during the changing of the frequency, and since these values are provided at 10 kHz, from the table is possible to accept that the values remail almost the same sin we are working at 16kHz. This kind of graph that put in relation the parameters with the frequency are missing in the datasheet that are chosen but from different manufacturer it was possible to very this assumption and take it as general rule for the industry:



Different is for the relation that link some characteristic with temperature, unfortunately not all the graph are present for every parameter but is possible to have an idea from the following examples





It is possible to directly estimate the relation between the maximum current and the ambient temperature that is also reflect on the maximum overtemperature that is possible to reach without corrupting the value find on the datasheet.

It is also possible to consider these values constant for this design, but in a deeper analysis can be implemented only by experimental simulation.

Output capacitors

Independently from the control method used to for drive the boost stage, the output capacitor show a voltage ripple at twice the line frequency. This behavior helps to provide an average output power that is almost constant if also the ripple is constant, otherwise it contains a ripple at twice the line frequency.

The design of this capacitor start from the evaluation of the powers that take part in this system: by doing an energy balance (starting from the powers) between the energy variation of the output capacitor and the input grid energy while it is considered a PF ~=1.

$$\Delta E_{g,AC} = \Delta E_c$$

$$\frac{P_o}{\omega_g} = \frac{1}{2} C_{DC} \left(V_{o,avg} + \frac{V_{rip}}{2} \right)^2 - \frac{1}{2} C_{DC} \left(V_{o,avg} - \frac{V_{rip}}{2} \right)^2$$

and the energy variation of the AC greed
formula

by force them to be equal it is possible to obtain a formula for the required output capacitance

$$C_{DC}^{*} = \frac{P_o}{\omega_g V_{o,avg} V_{rip}}$$

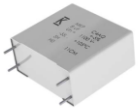
with this value it is possible to sustain the predicted ripple.

It's interesting to notice that this value is a way lower than the output capacitance that is required in a bridge rectifier. So by having the same output we can choose a lower and more compact capacitance.

	C_{DC}	
Bridge rectifier	0.007676907889681 F	x5
PFC	0.001514859660601 F	x1

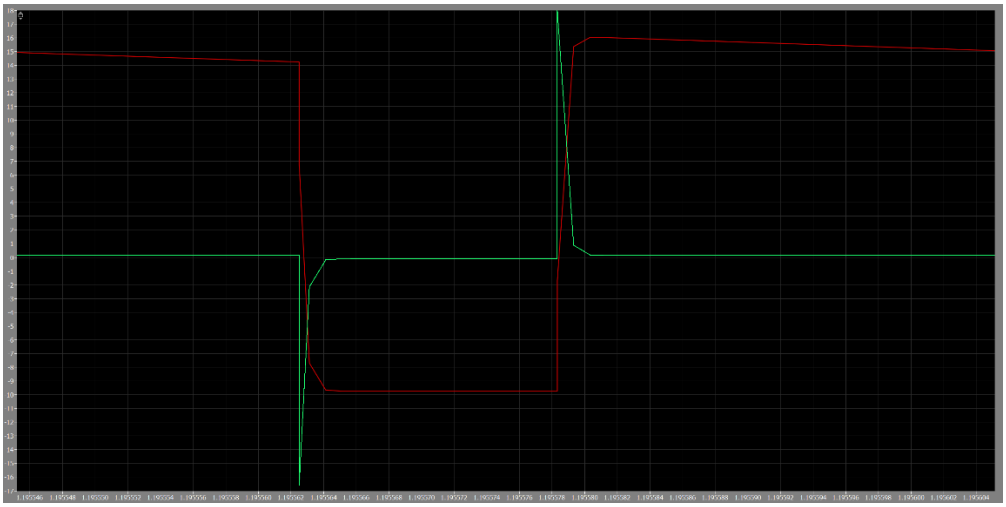
Rated Voltage	Rated Capacitance	Size Code	Case Size	Ripple Current		ESR Maximum	Impedance Maximum	Part Number
500	1,600	FP	45 x 105	6.09	11.29	144	107	ALC70(1)162FP500

A good choice is to divide the output capacitance in two parallel capacitance one that represent by a bulk capacitor with an high value of charge and it contribution is dominant in low frequency , while the other one is chosen to be around 1% of the charge of the bulk one and it is contribution is crucial in high frequency.



Cap Value (µF)	VDC	Dimensions (mm)					dV/dt	Ipkr	ESL	ESR 70°C at 10 kHz	Irms* 70°C at 10 kHz	Rth (HS/Amb)	Packaging Quantity	PART NUMBER
		T	H	L	S	S1	V/µs	Apk	nH	mΩ	Arms	(°C/W)		
V_{NDC} at 70°C = 500 VDC; V_{OP85} at 85°C = 450 VDC; V_{OP105} at 105°C = 350 VDC														
5.6	500	11	20	31.5	27.5	\	10	54	17	12.7	6.8	44	256	C4AQLBU4560A1WK
10	500	13	25	31.5	27.5	\	10	96	22	7.8	9.6	36	234	C4AQLBU5100A1XK
12.5	500	14	28	31.5	27.5	\	10	122	24	6.7	11.0	33	96	C4AQLBU5125A1YK
15	500	19	29	31.5	27.5	\	10	147	25	5.8	12.6	29	72	C4AQLBU5150A11K

The current is shared among the capacitors according to their inductances. The high frequency bypass capacitor provides the largest part of the current during switching transient, around the 86%. There is to take into account that a large current derivative can lead to a voltage overshoot that can damage the device. After the switch event the bulk capacitor recharge the HF one and it operate providing the AC component of the current for almost all the remain part of switching period.



Since during the transient the contribution to the over voltage of the transistor is up to the high frequency bypass capacitor, is fair to underline that for a silicon carbide and GaN transistor is required an optimization of all the component of the switching cell because by increasing the derivative is also possible to obtain a different voltage overshoot value and there topology is built to be limited in the value of the rise and the fall, that will be a way shorter for wide band gap devices. It require a lower inductance of the bypass capacitor since is needed to reduce the voltage stress on the transistor, moreover the resonant frequency of the bulk capacitor should be much greater than the switching frequency of the compensator because we are going to work with higher value of switching frequencies.

Inductances

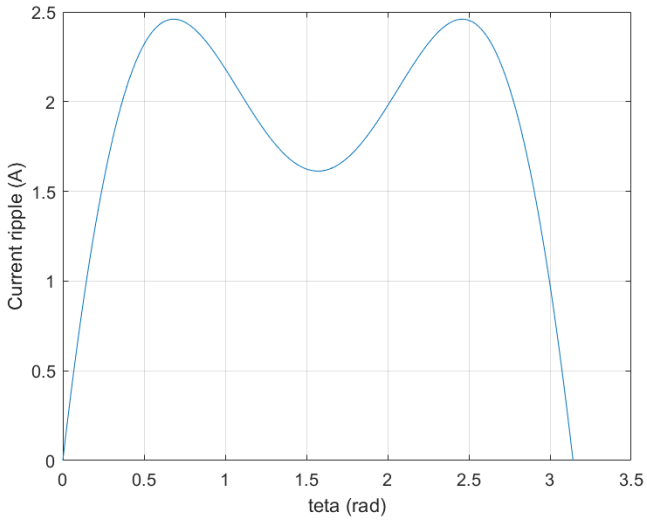
A part from the stray inductances of the single devices, in this model are present 2 main inductances. The one that represent the stray inductance, and it is important to have a more realistic grid and the one from the boost cell.

They boost inductance is the inductance that contribute to the boost stage. The design of this component is devolved to limit the high frequency current ripple. The current of the inductor is made-of two parts: the low frequency component and the high frequency one.

$$i_L = \frac{2P_0}{V_{gM}}\left|\sin\vartheta\right| + \Delta i_L$$

by analyzing the high frequency component is possible to notice that the ripple is not constant during the period, so it is important to understand where is placed the maximum.

$$\Delta i_L = \frac{V_{gM}\left|\sin\vartheta\right|}{LF_{sw}}\left(1-\frac{V_{gM}\left|\sin\vartheta\right|}{V_o}\right) \qquad \frac{d\Delta i_L}{d\vartheta} = \frac{d}{d\vartheta}\left[\frac{V_{gM}\left|\sin\vartheta\right|}{LF_{sw}} - \frac{V_{gM}^2\left|\sin\vartheta\right|^2}{V_o LF_{sw}}\right] = 0$$



Once I have found the maximum angle it is possible to have a lower limit of the desired boost inductance that is needed to reduce the ripple.

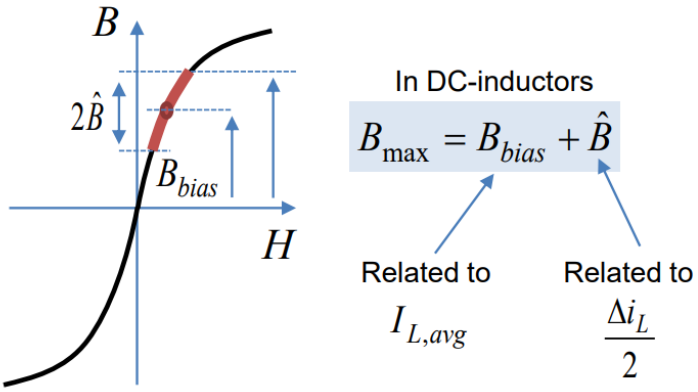
$$L \geq \frac{V_{gM}\left|\sin\vartheta_{\max}\right|}{\Delta i_{L,\max} F_{sw}}\left(1-\frac{V_{gM}\left|\sin\vartheta_{\max}\right|}{V_o}\right)$$

Now with these raw value is important to start a proper design workflow because the inductances are not already made but can be obtained by choosing a proper core and then let the manufacturer do the winding of the coils and after that provide to the customer the inductor with package included.

Their first step to follow is to collect all the data specifics of the inductor such as:

switching frequency, minimum inductance value, RMS value of the current come the current ripple, the average value of the current.

To start the research on the datasheet, the first step to do is to look at the core behavior in terms of magnetic properties. In this project is required a DC inductor (DC choke) because the shape of the current waveform is affected by a bias component plus a ripple (low+high frequency).This behavior is reflected on the magnetic flux that is composed by an AC component plus a bias.



Now by looking to the catalogue data with the test condition is possible to choose a proper value of the magnetic flux. This step is important because the maximum value of the flux density reached in our core is part of the formula that allow us to find a proper corner. In this case since the working frequencis low, Bmax is only limited by the saturation of the material and not from the core losses. ($B\_\max = B_{sat} \sim 0.35\,T$)

The formula of the product area Ap is useful to find a right core in the datasheet:

$$A_p = A_w A_c = \frac{L i_{L,RMS} i_{L,\max}}{k_w B_{\max} J}$$

Having Ap=120.306 (cm^4), the ferrite toroid that was on some datasheet had to much difference in terms of AP so the only one that fit with this constrain was the Ferrite U shape with an of Ap=121 (cm^4) that is perfect for this design.

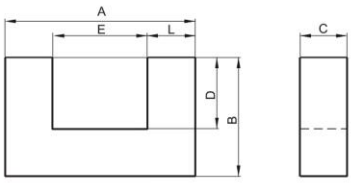
MAGNETICS
A Division of Spang & Company

Specification for:

0P49925UC

110 Delta Drive
Pittsburgh, PA 15238
Phone: 412/696-1333
Fax: 412/696-0333
Email:magnetics@spang.com

DIMENSIONS



(mm)	Nominal:	Tol. min.:	Tol. max.:
A	101.6	-1.5	+ 1.5
B	57.1	-0.4	+ 0.4
C	25.4	-0.6	+ 0.6
D	31.7	-0.75	+ 0.75
E	50.8	-1.0	+ 1.0
L	25.4	-0.8	+ 0.8

Eff. Parameters			
Ae mm ^{2}	Amin mm ^{2}	le mm	Ve mm ^{3}
645.0	645.0	308.0	199000

INDUCTANCE

AL value (nH/T^2)	Test conditions
Nom: 5500±25%	10 kHz, < 0.5 mT, 25 °C

MARKING

0P49925UC
PXXXXX

CORE LOSSES

P, max	Test conditions
< 32 W/set (< 161 mW/cm^3)	100 kHz, 100 mT, 100 °C

NOTE

Spec. modifications	Previous	Revised
2005-11-21	B=56.8 Min. D=31.1 Min. Losses: General P material	B=56.7 Min. D=30.95 Min. Losses: Detail as indicated
2010-09-27	Al.4920 Nom Al.3650 Min.	Al.5500±25%

Now by doing some calculation is possible to obtain the windows area and the cross section area

```
Ap_new
```

```
Ap_new = 1.2100e-06
```

```
Ac
```

```
Ac = 6.4500e-04
```

```
Aw=Ap_new/Ac
```

```
Aw = 0.0019
```

Is possible to obtain the number of the turns of the coil and other parameters like the diameter of each wire (from a catalogue) and also the DC resistance that is going to be integrated in the circuit

```
N=L*iL_max/(Ac*B_sat)
```

```
N = 273.1346
```

```
N_new=round(N)
```

```
N_new = 273
```

```
R_DC_L=N_new*rho_Cu_20*l_mean/A_cu
```

```
R_DC_L = 0.2065
```

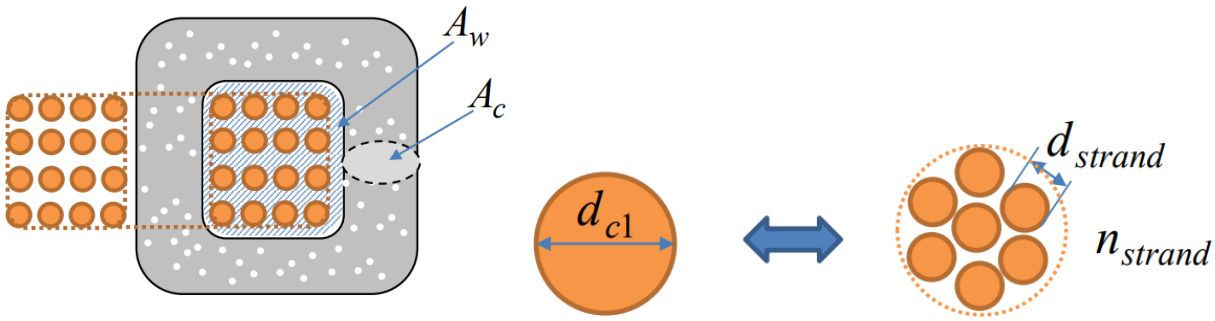
```
A_cu=Aw*kw/N_new
```

```
A_cu = 2.7487e-06
```

```
dw_cu=sqrt(4*A_cu/pi)
```

```
dw_cu = 0.0019
```

```
%from catalogue
dw_cu_new=0.002;
```

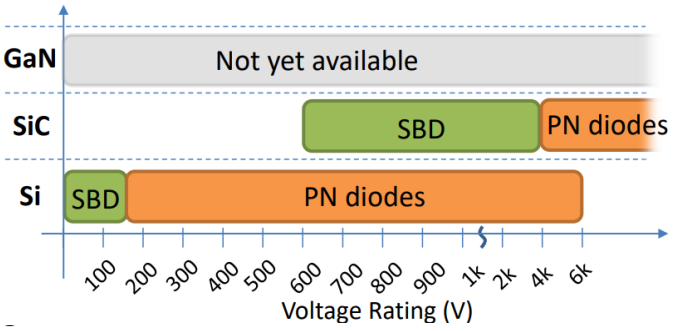


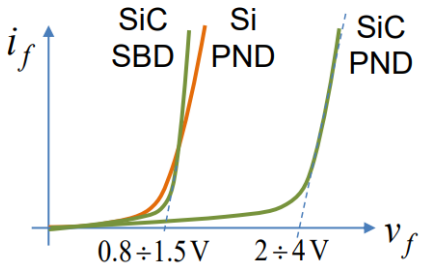
Choice of active device

Diode

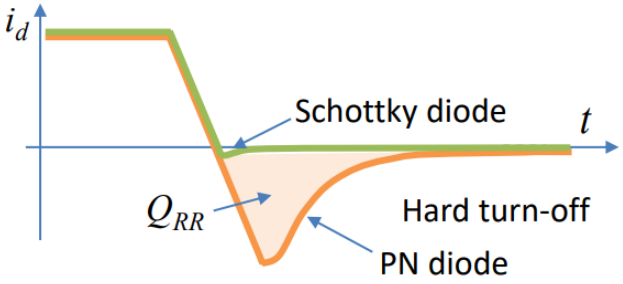
In this scheme are present numerous diodes. The diode bridge rectifier is made of four diode. The rating voltage is above the 100 V, this lead to the exclusion of the Silicon SBD even if they are not even necessary in this specific application since the switching losses are low enough to be able to accept the losses coming from the irreversible charge that of PN diode since each diode switch only two time every grid period. The best choice is related to PN Si diode, since the working frequency are not so high to be forced to choice a SiC configuration because from the dynamic and losses point of view there are not so evident advantages against the high cost that it would mean.

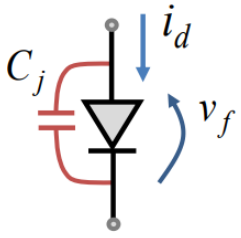
(Having an higher bandgap lead also to an higher threshold voltage, that increase a lot the conduction losses, that is why the wide bandgap devises should be employed only is high voltages and frequency are needed)





Lower reverse recovery charge





This rule is also valid for the boost diode. In fact all the 5 diode present in the scheme are from the same topology and also with the same characteristic. This diode is

operating at higher frequency than the ones in the bridge, so a SiC configuration in this case could be a good choice but from the simulation the losses introduced from the Si component are acceptable and this justify the choice of using a lower price component .To obtain higher efficiency a SiC is needed for the boost diode.

IDFW40E65D1E

Emitter Controlled Diode Rapid 1 Advanced Isolation

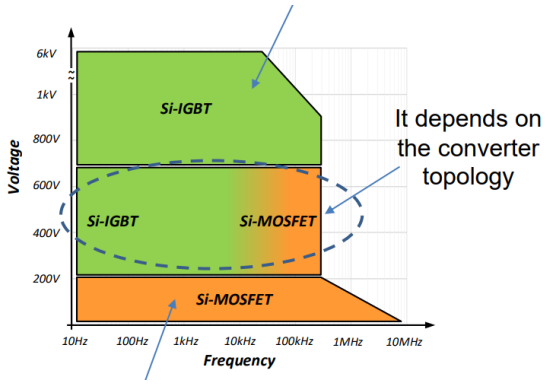
Maximum Ratings

For optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

Parameter	Symbol	Value	Unit
Repetitive peak reverse voltage, $T_{vj} \geq 25°C$	V_{RRM}	650	V
Diode forward current, limited by T_{vjmax} $T_h = 25°C$ $T_h = 65°C$	I_F	 42.0 35.0	A
Diode pulsed current, t_p limited by T_{vjmax}	I_{Fpuls}	120.0	A
Power dissipation $T_h = 25°C$ Power dissipation $T_h = 65°C$	P_{tot}	78.0 57.0	W
Operating junction temperature	T_{vj}	-40...+175	°C
Storage temperature	T_{stg}	-55...+150	°C
Soldering temperature, wave soldering 1.6mm (0.063in.) from case for 10s		260	°C
Mounting torque, M3 screw Maximum of mounting processes: 3	M	0.6	Nm
Isolation voltage RMS, $f = 50/60Hz$, $t = 1min$[1)]	V_{isol}	2500	V

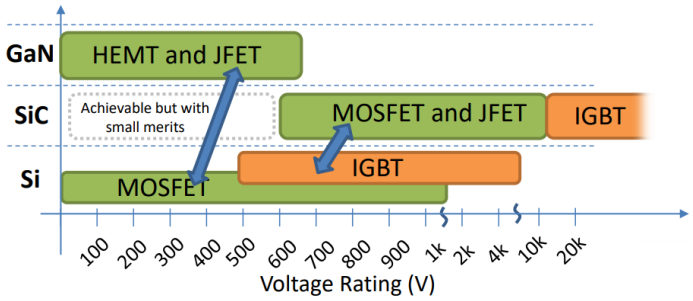
Transistor

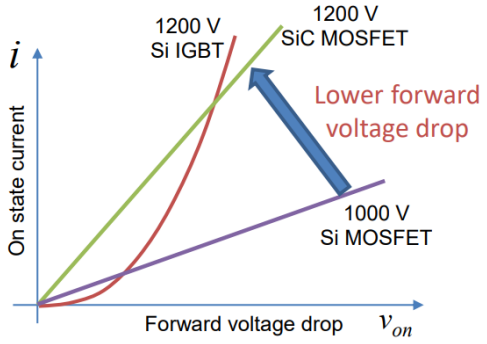
The transistor placed in the boost stage, require to be able to switch at 16 kHz frequency but at the same time it should be able to sustain voltage around 410 V. This specifics are typical of the border line region in which it is possible to choose both a Si MOSFET or an IGBT.

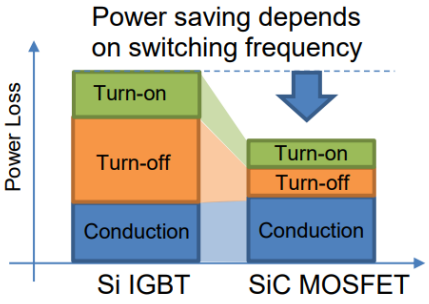


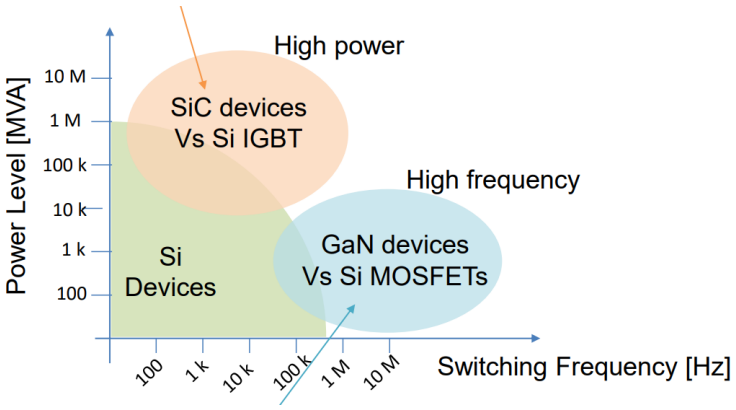
To consider the higher switching losses that an IGBT can experience , it is better to choose a MOSFET.

For the semiconductor technology, is fair to underline that the SIC MOSFET are mainly used in higher voltage rating and when the conduction losses of the MOSFET became to high and instead of using an IGBT (if possible) the SiC MOSFET can be the best compromise. All the discussion about the semiconductor done for the diodes is also valid here, but mainly in this type of configuration both Si MOSFET and Si IGBT can be chosen since with both of them is possible to obtain the constrain imposed for the project, by maintaining a good efficiency.

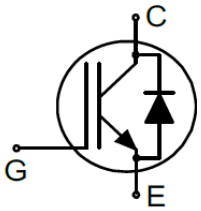








The chosen IGBT is the following, the datasheet also describe the external diode that in this sample is packed directly with the transistor.



AIKW50N60CT

TRENCHSTOP™ Series

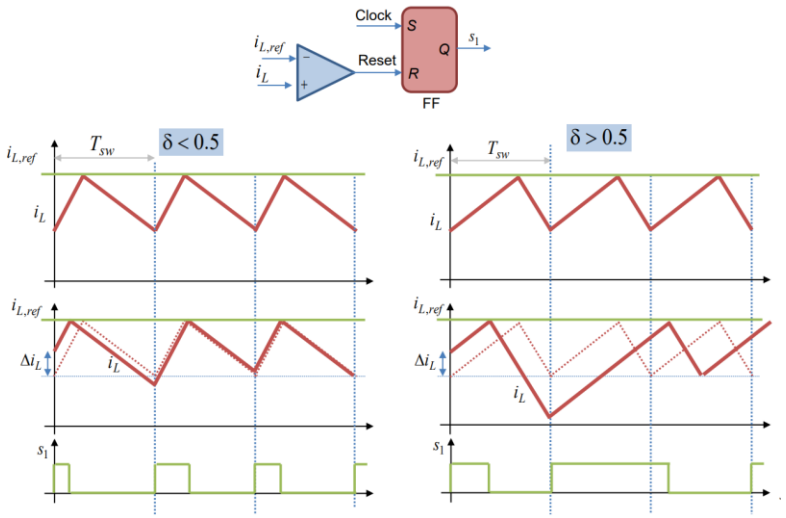
Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage, $T_{vj} \geq 25°C$	V_{CE}	600	V
DC collector current, limited by T_{vjmax} $T_C = 25°C$ value limited by bondwire $T_C = 100°C$	I_C	 80.0 50.0	A
Pulsed collector current, t_p limited by T_{vjmax}	I_{Cpuls}	150.0	A
Turn off safe operating area $V_{CE} \leq 600V$, $T_{vj} \leq 175°C$, $t_p = 1\mu s$	-	150.0	A
Diode forward current, limited by T_{vjmax} $T_C = 25°C$ value limited by bondwire $T_C = 100°C$	I_F	 80.0 50.0	A
Diode pulsed current, t_p limited by T_{vjmax}	I_{Fpuls}	150.0	A
Gate-emitter voltage	V_{GE}	±20	V
Short circuit withstand time $V_{GE} = 15.0V$, $V_{CC} \leq 400V$ Allowed number of short circuits < 1000 Time between short circuits: ≥ 1.0s $T_{vj} = 150°C$	t_{SC}	 5	µs
Power dissipation $T_C = 25°C$	P_{tot}	333.0	W
Operating junction temperature	T_{vj}	-40...+175	°C
Storage temperature	T_{stg}	-55...+150	°C
Soldering temperature,[1] wave soldering 1.6mm (0.063in.) from case for 10s		260	°C
Mounting torque, M3 screw Maximum of mounting processes: 3	M	0.6	Nm

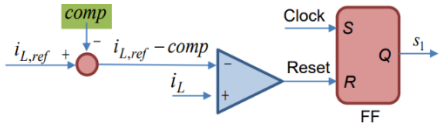
Control strategy

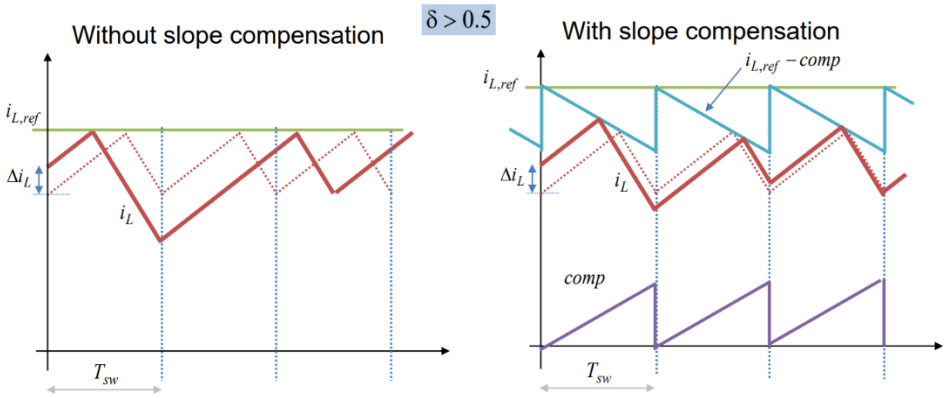
The control scheme for the boost stage consist in a cascade loop, it is made of two loops: the external loop that controls the average output voltage. Than the voltage regulator ask for different current level, the voltage error becomes a reference in terms of current. This current must be controlled in order to have exactly the reference current in the circuit and then is possible to control the gate signal of the transistor.

For this topology there are numerous control strategy that can be implemented, the most known are : the peak current control, the average current mood, the austerities current control and the critical current control. Among these, it was chosen the peak current control because it has an easy and robust control of the current, is possible to have an high regulation of the dynamic; by introducing a compensation is possible to operate at constant switching frequency; it is possible to sense directly the switch current instead of the inductor current that should require an all effect sensor and it will introduce an higher degree of complexity. Unfortunately this technique is characterized by the high sensitive to the commutation noises, the shape of the input current is equal to the shape of the grid voltage, that means if the grid is distorted the converter absorbs at distorted current. And finally as previous anticipated, to overcome the subharmonic oscillation in the input current for a duty cycle greater than 0.5, a slope compensation ramp is needed, the amplitude of this ramp if is too large could distort the input current.



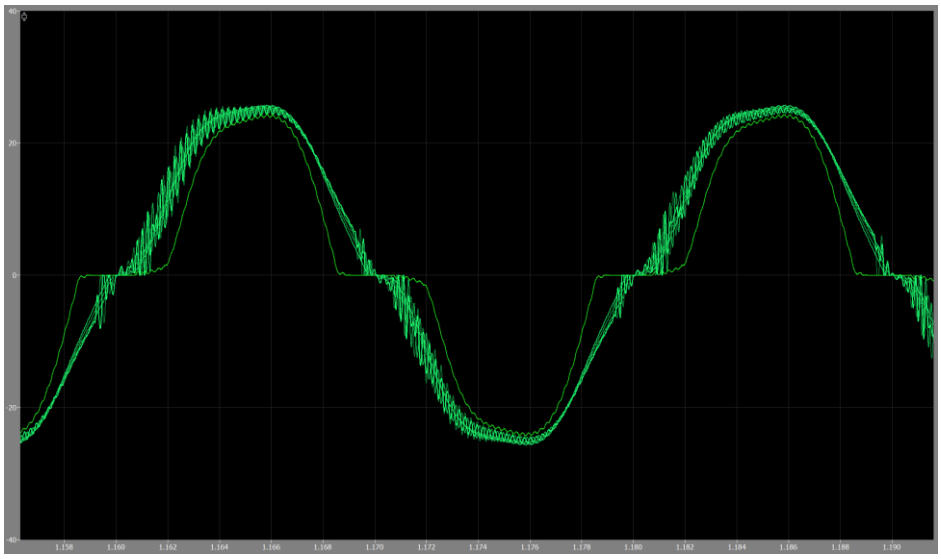
It is possible to substitute the boost inductor current reference with the current that



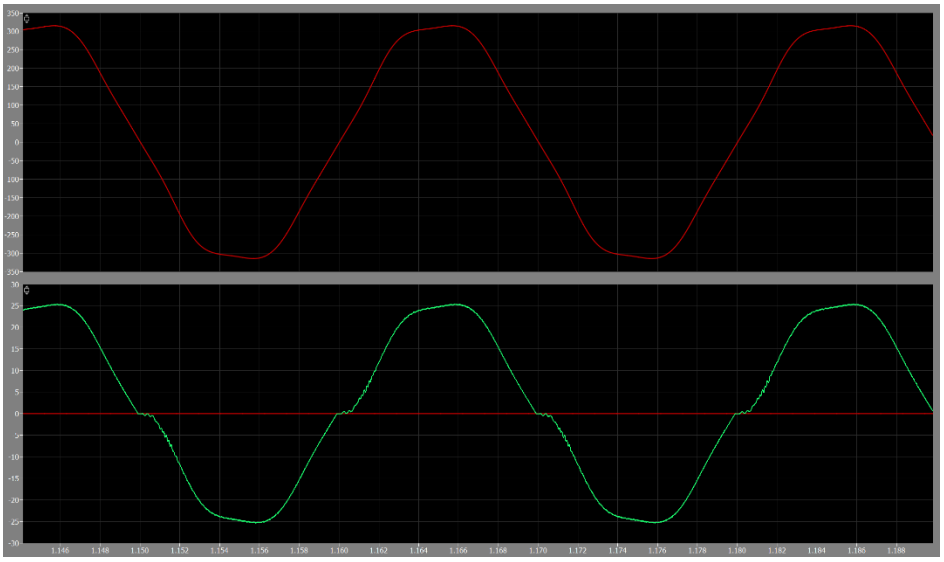


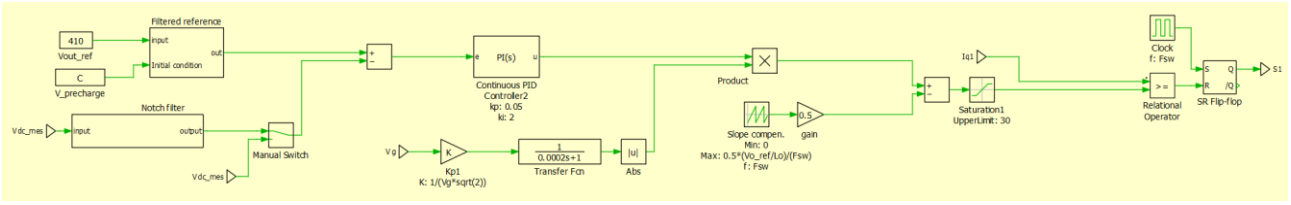
flow in the transistor.

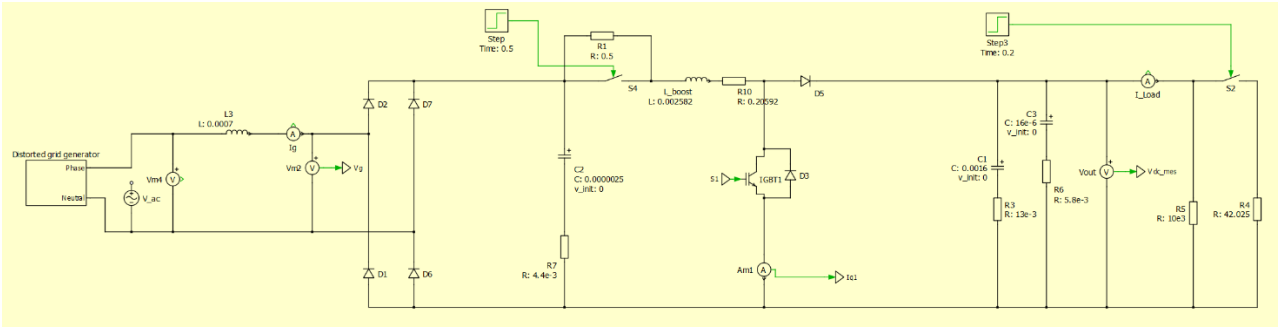
This is the result obtained by changing the magnitude of the saw tooth compensator, by increasing it is possible to reduce the peak current but the shape starts to became less sinusoidal (similar to the one of the bridge rectifier) but reducing the magnitude is possible to experience the skip of the period that lead harmonic disturbances.



Best result: (top: input grid voltage, bottom: input grid current)

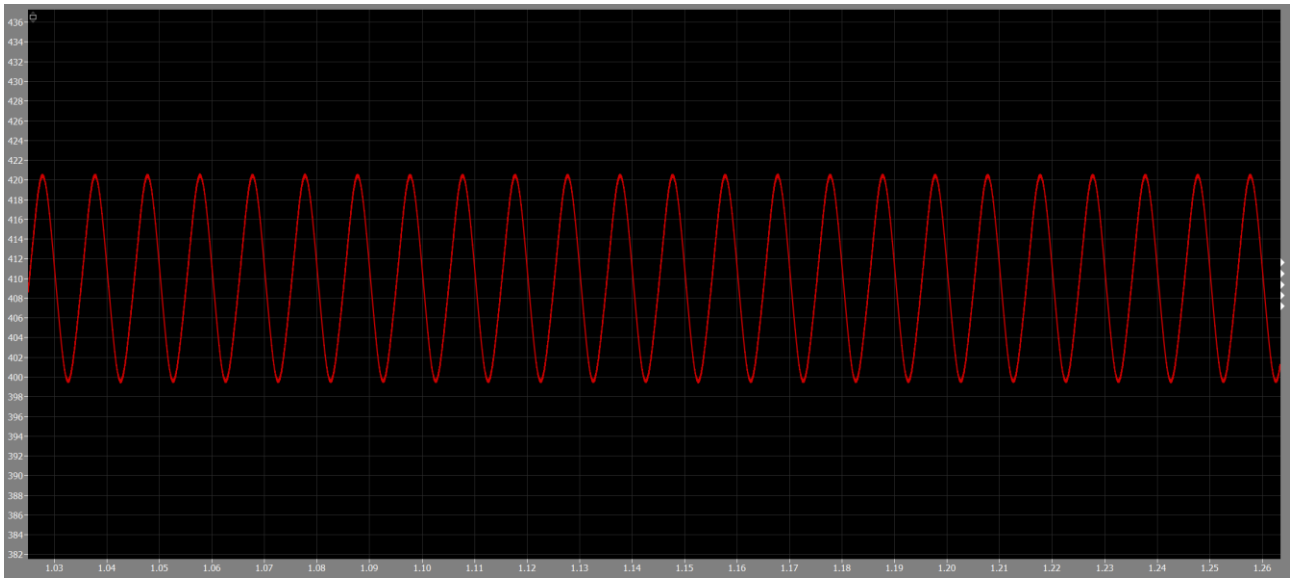




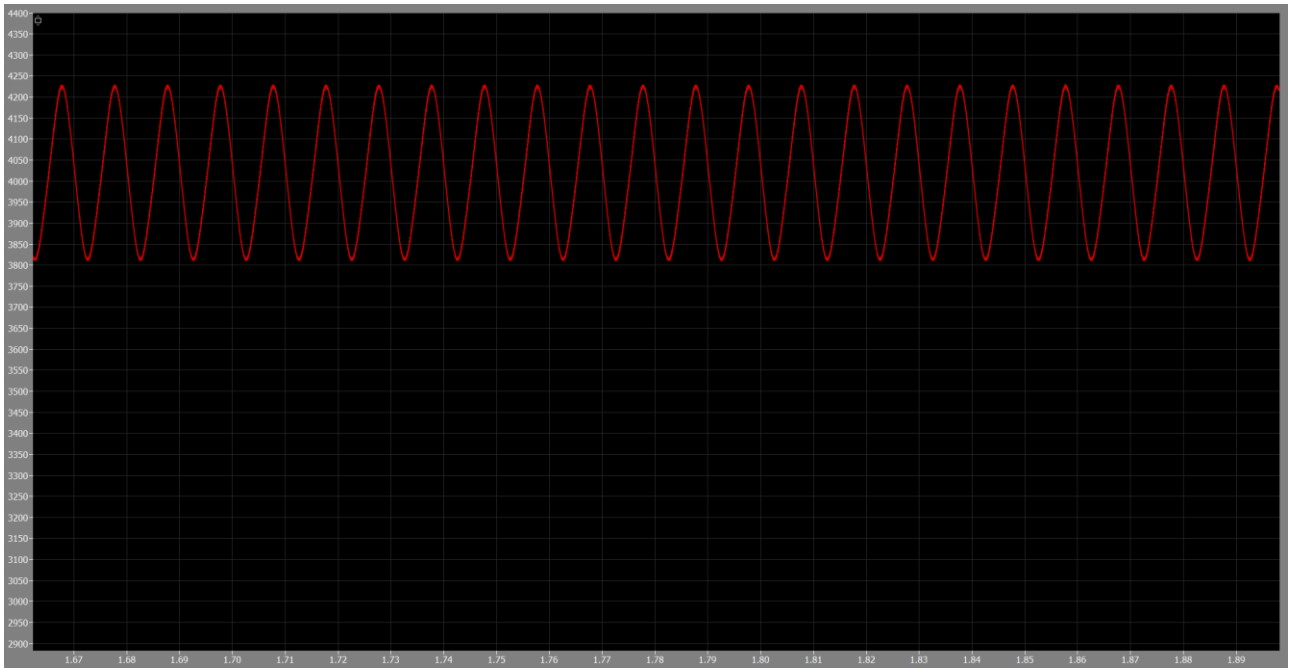


Results

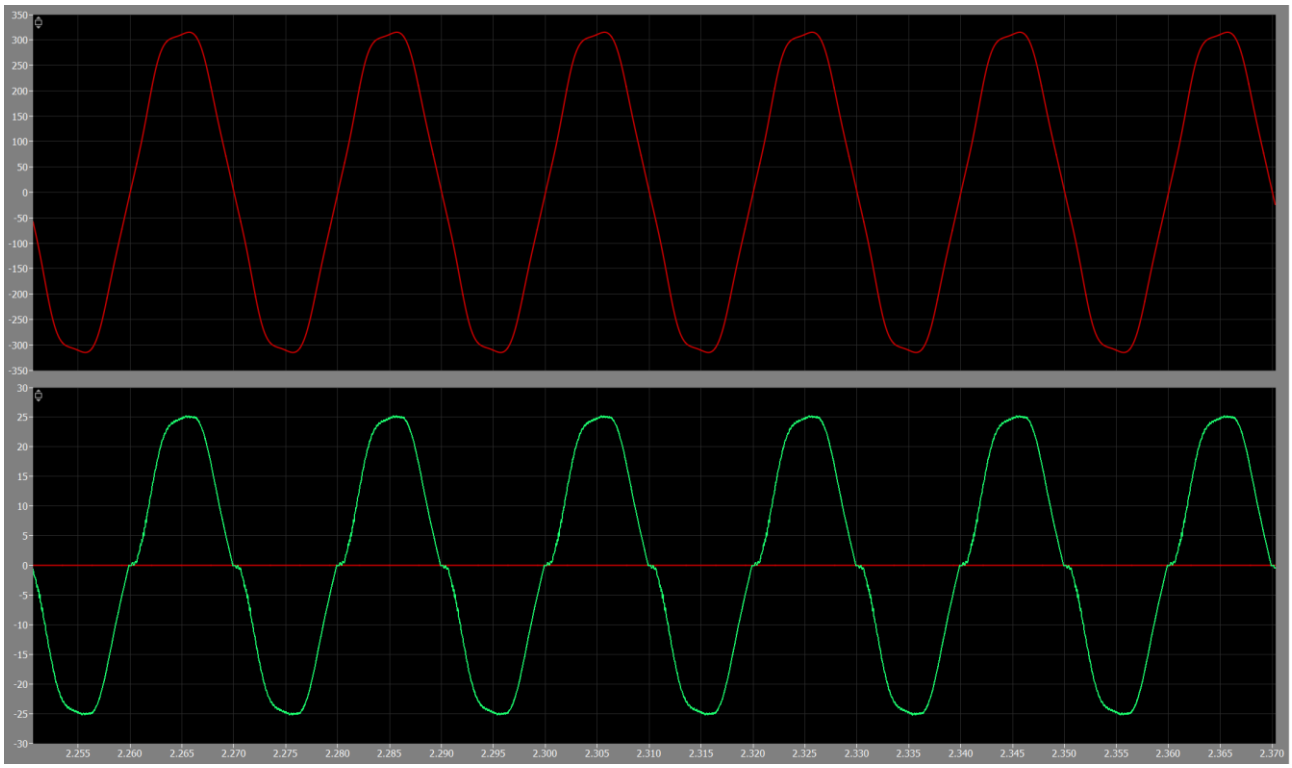
Output voltage:



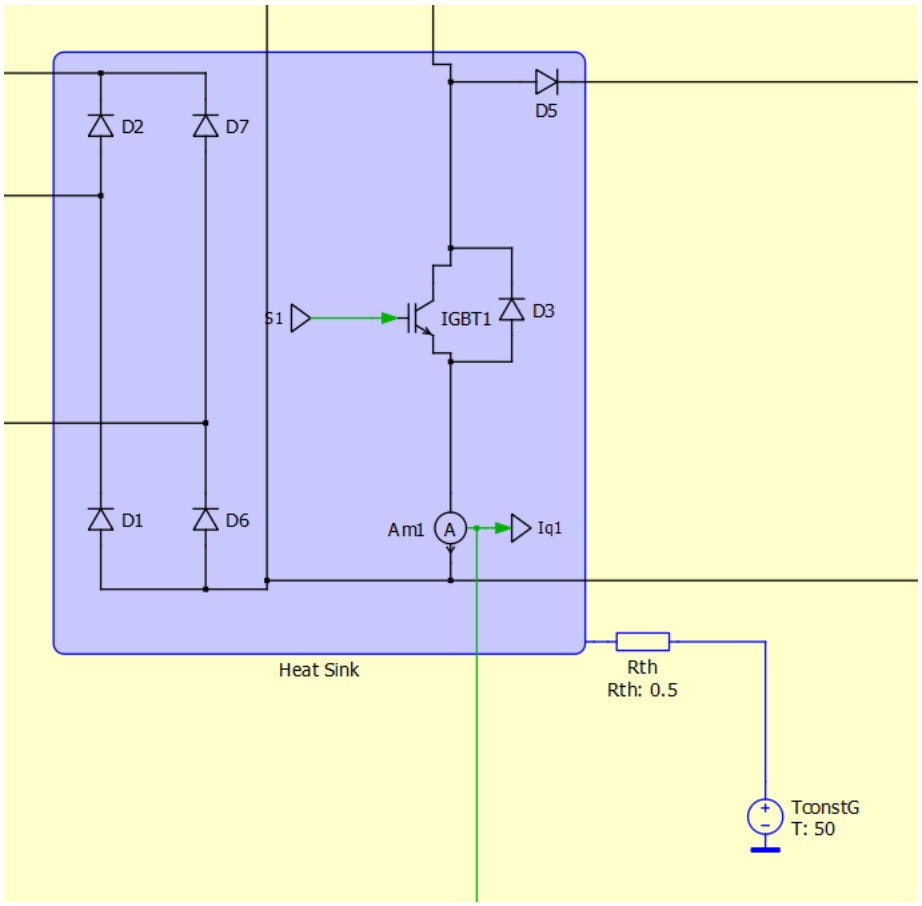
Output power



Input voltage and current

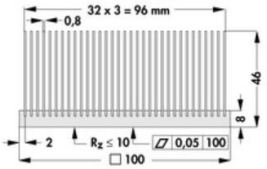


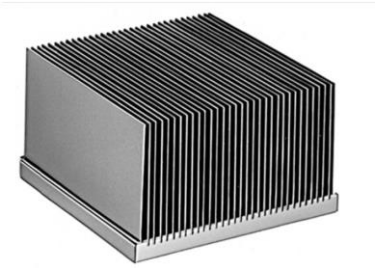
Thermal model



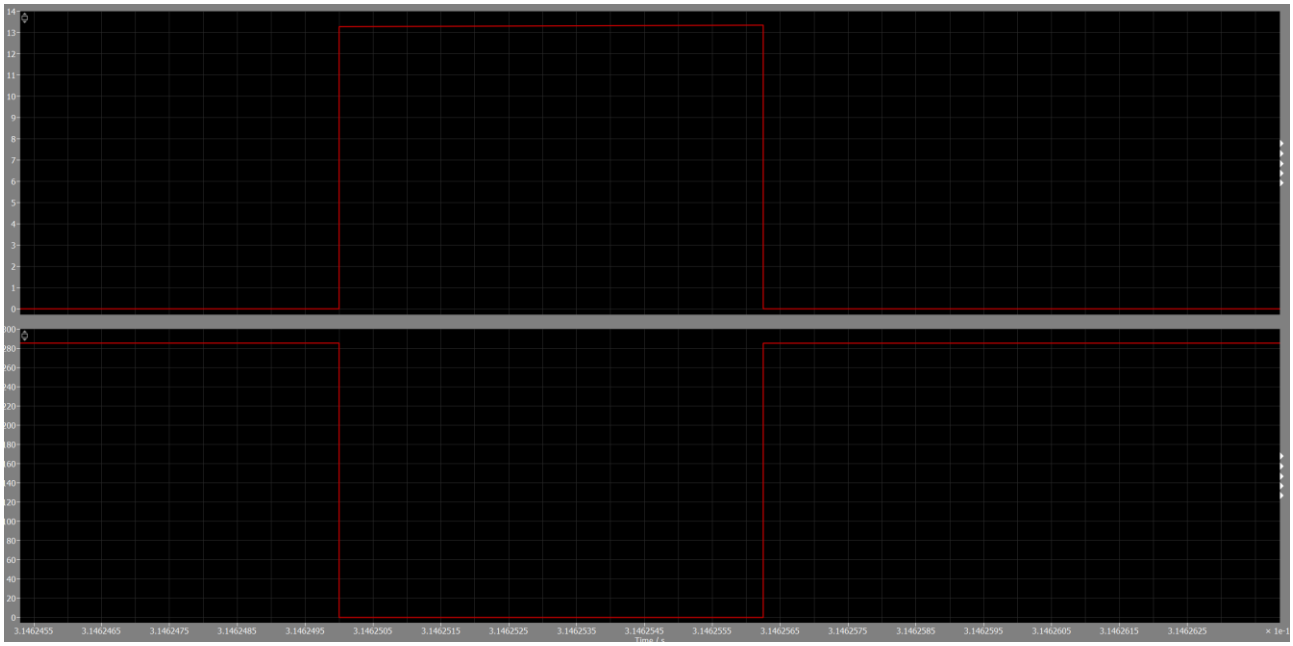
In order to provide good results the following analysis it was done by considering simultaneously two different situation, one in which the characteristic all of the devices should be extract from the datasheet and manually insert in the lookup table of the simulator and the other one that use readymade lookup table done by the company specifically for PLECS. The differences between these two are that the one provided by the manufacturer can provide a larger number of point that lead to a better approximation of the thermal behavior, the other one have pretty similar result but with lower number of point that introduce some approximation and moreover the switching losses of the diode in the bridge are considered negligible since the data sheet do not provide the plot needed to build the chart.

For this type of simulation it was considered an heat sink with a 1.5 K/W of thermal resistance and this value was improved also in accord to the results obtained by the first simulation and the heatsink available in the market. Only active component are under investigation and the passive one are considered ideal (do not affected by temperature drift neither source of it)





Since there is no overlap between the current and voltage (ideal transition) ,of the switching devices during the turn on and the turn off. The way implemented in PLECS to evaluate losses is based on look up table.



Ideal switching event

This table are based on the data provided by the manufacturer.

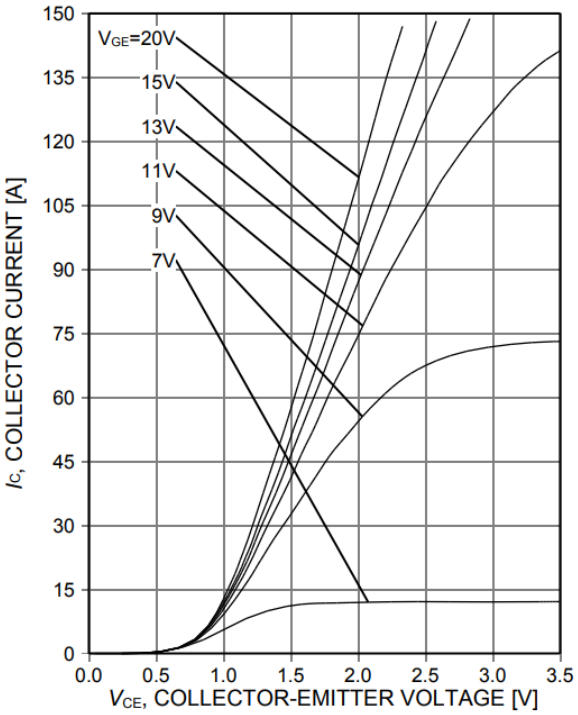


Figure 3. **Typical output characteristic** (T_j=25°C)

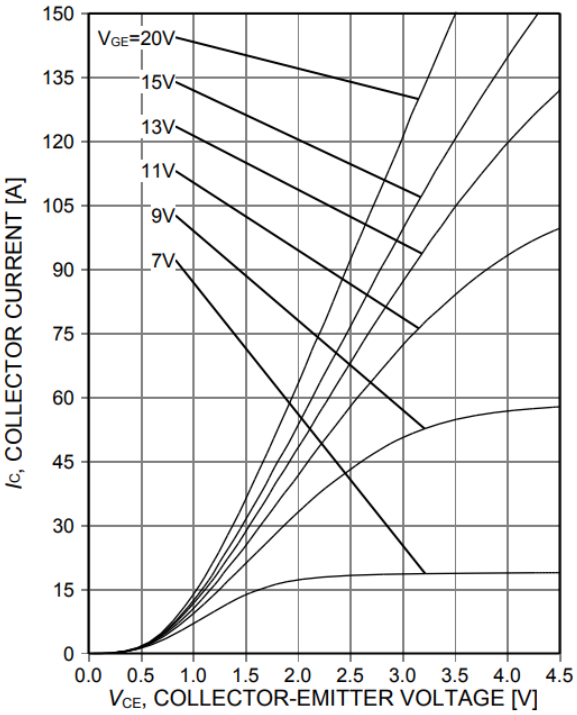
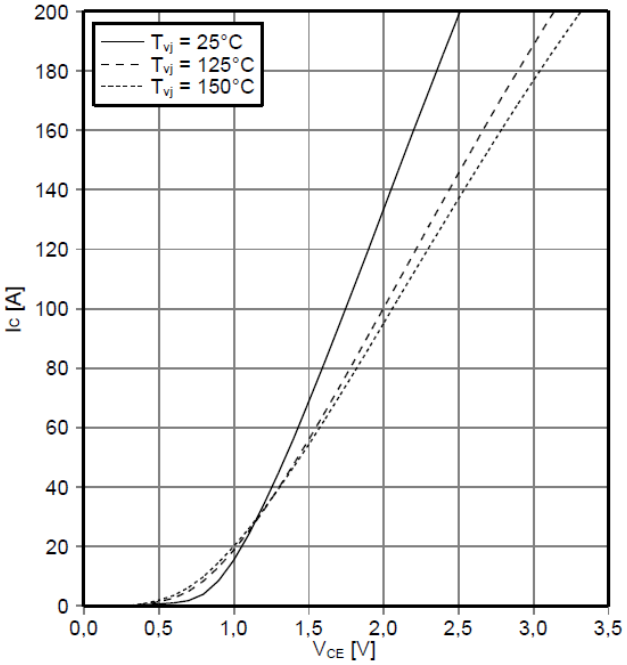
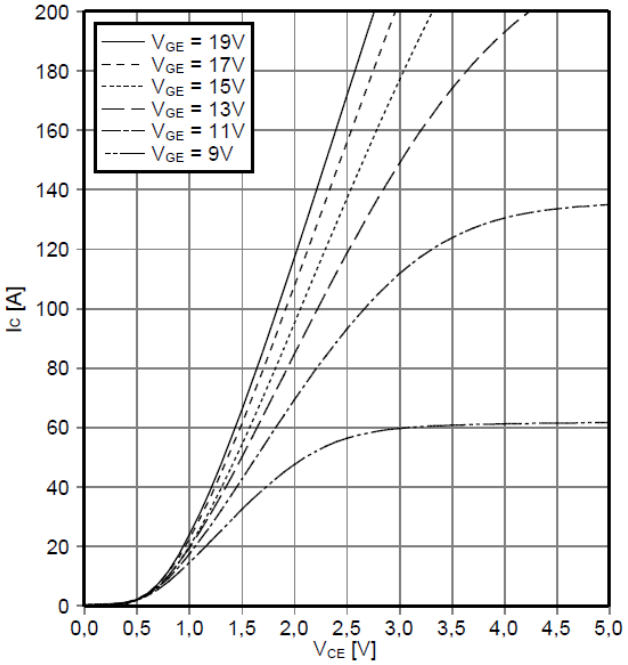


Figure 4. **Typical output characteristic** (T_j=175°C)

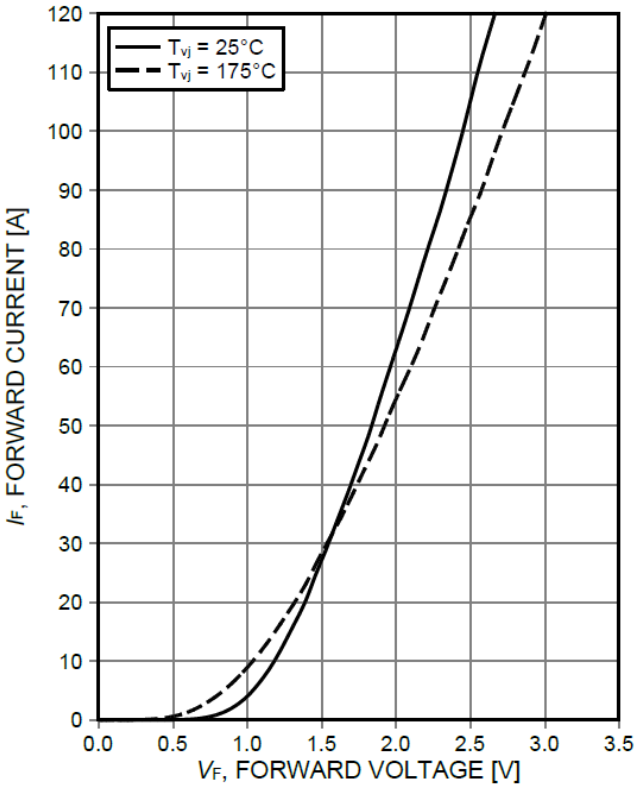
Static characteristics of IGBT A



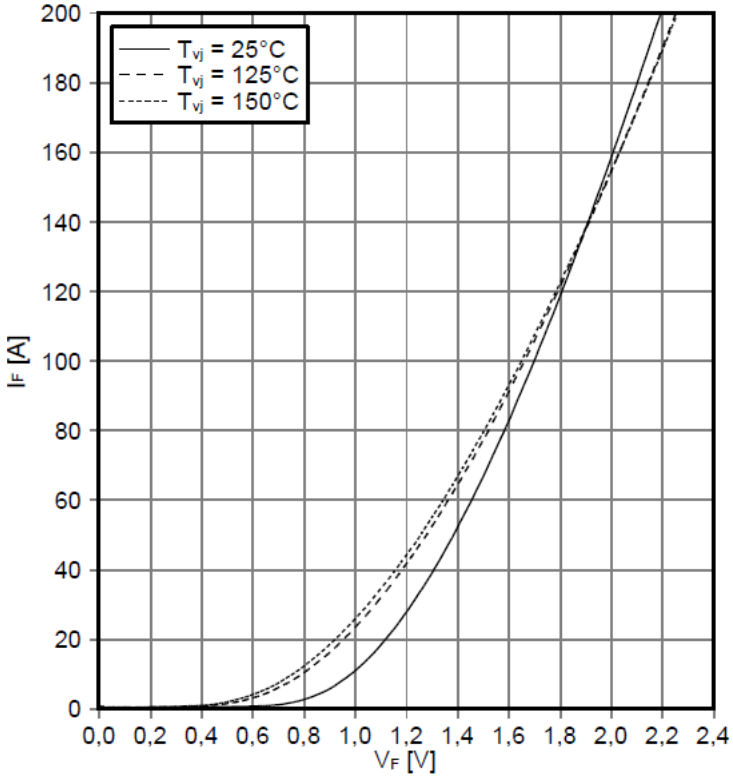


Static characteristics of IGBT B

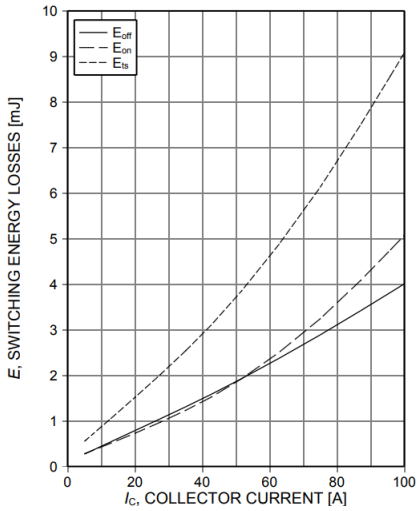
High voltage implies a more stable characteristic



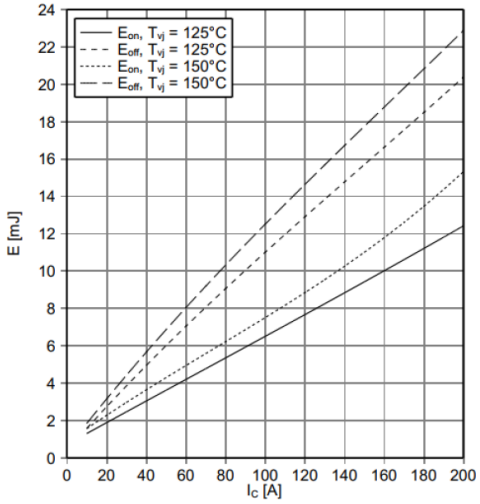
Static characteristic of Diode A



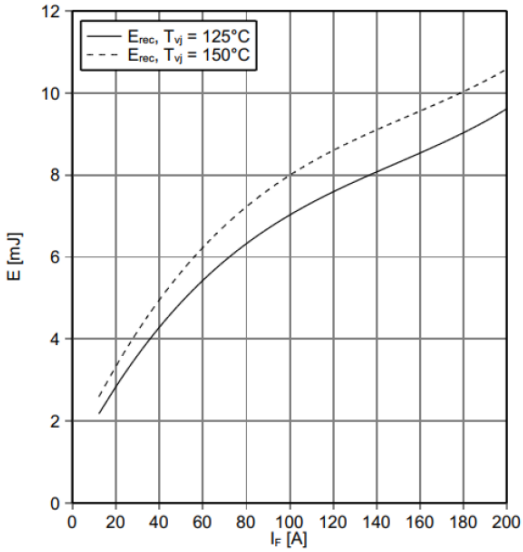
Static characteristic of Diode B



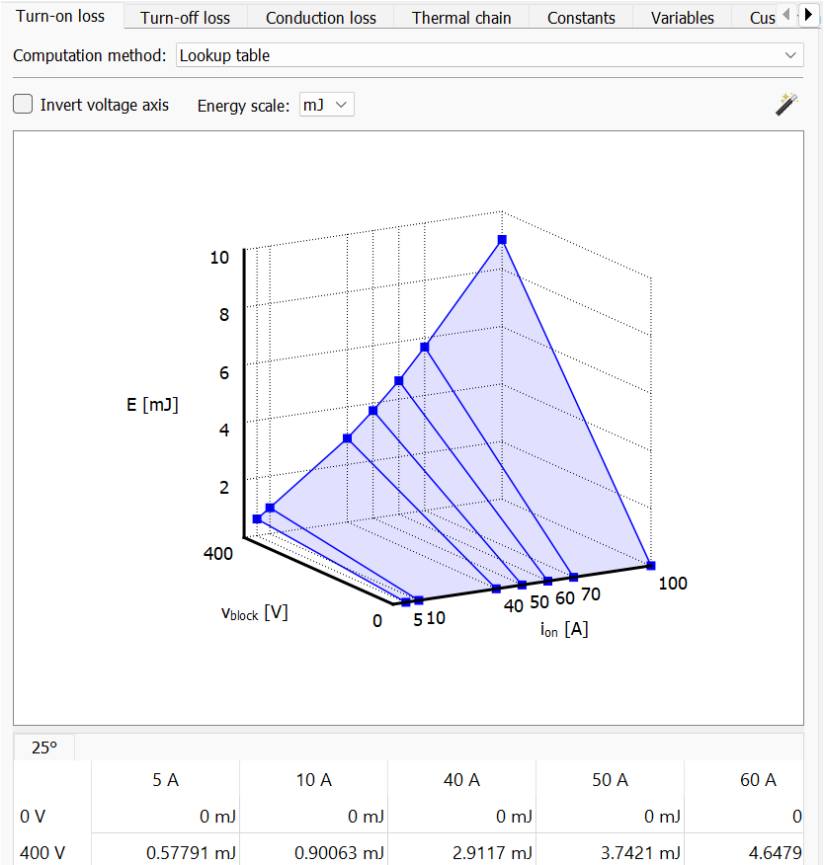
Dynamic characteristic A



Dynamic characteristic B



Dynamic characteristic B Diode



25°

	5 A	10 A	40 A	50 A	60 A
0 V	0 mJ	0 mJ	0 mJ	0 mJ	0
400 V	0.57791 mJ	0.90063 mJ	2.9117 mJ	3.7421 mJ	4.6479

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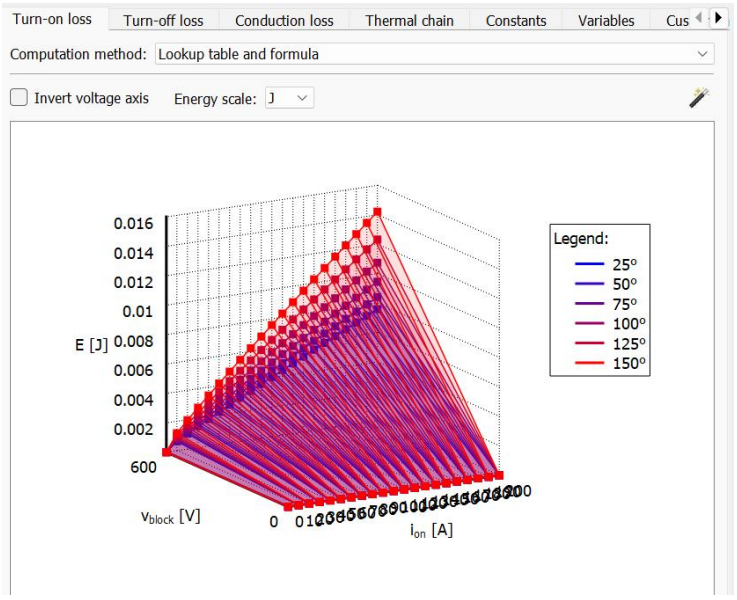

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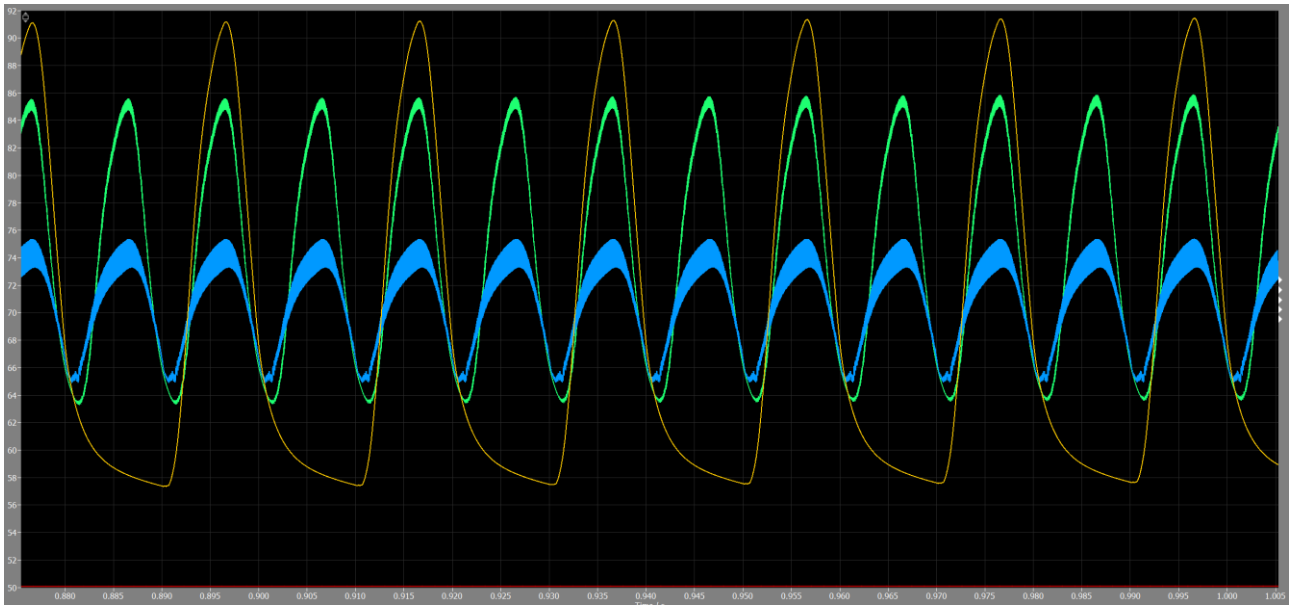
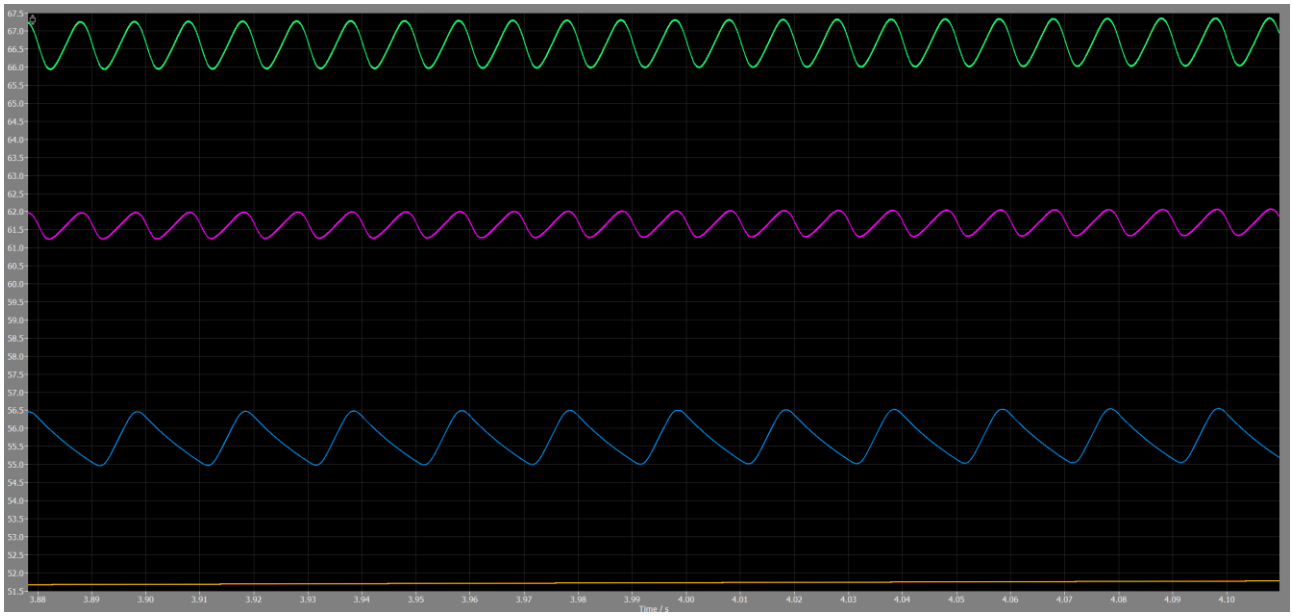
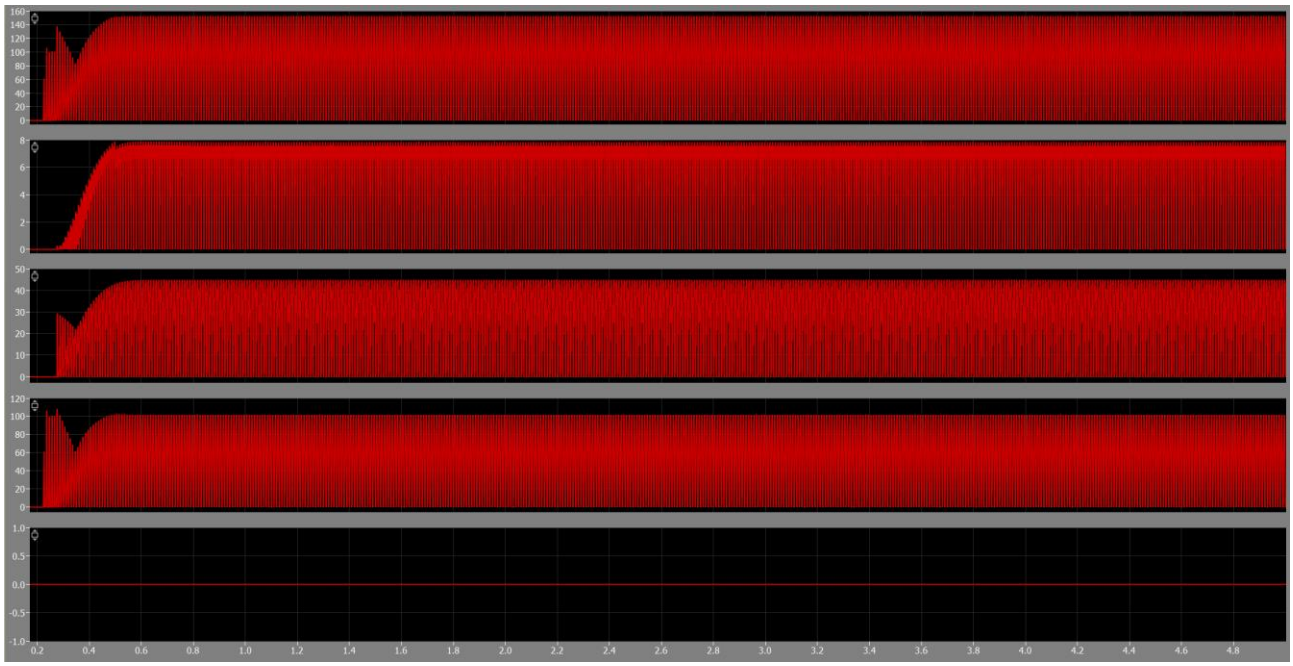
Junction temperature



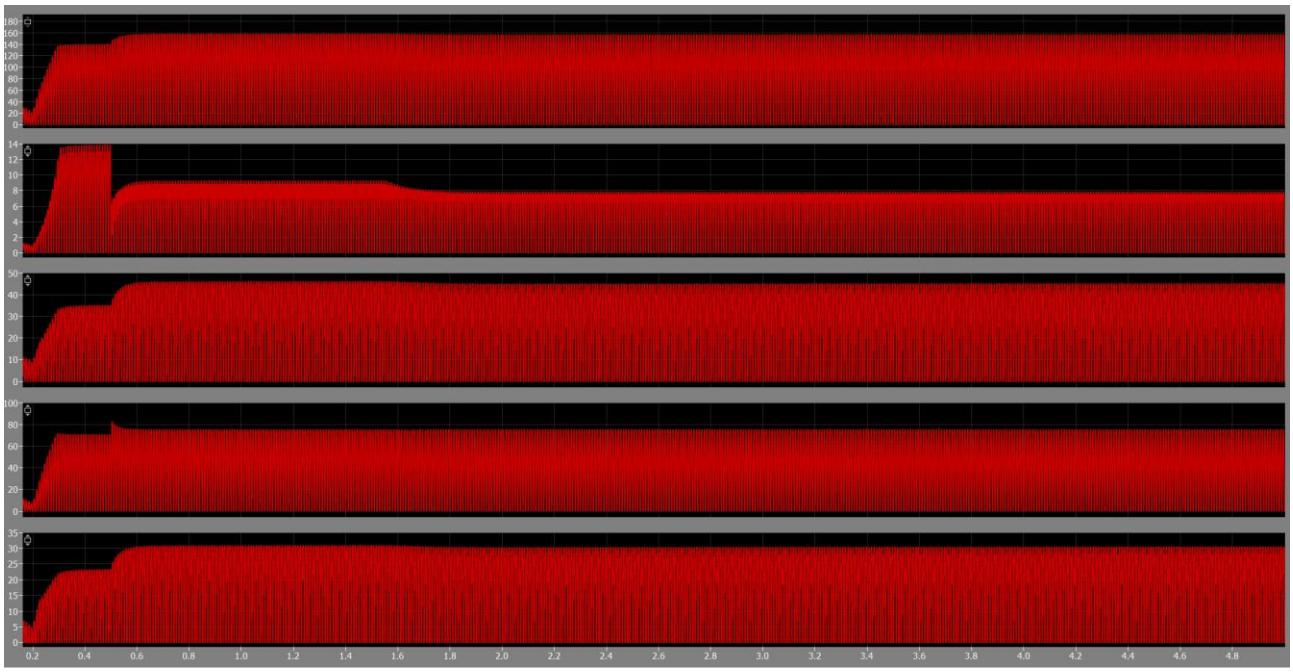
Vs



Total losses

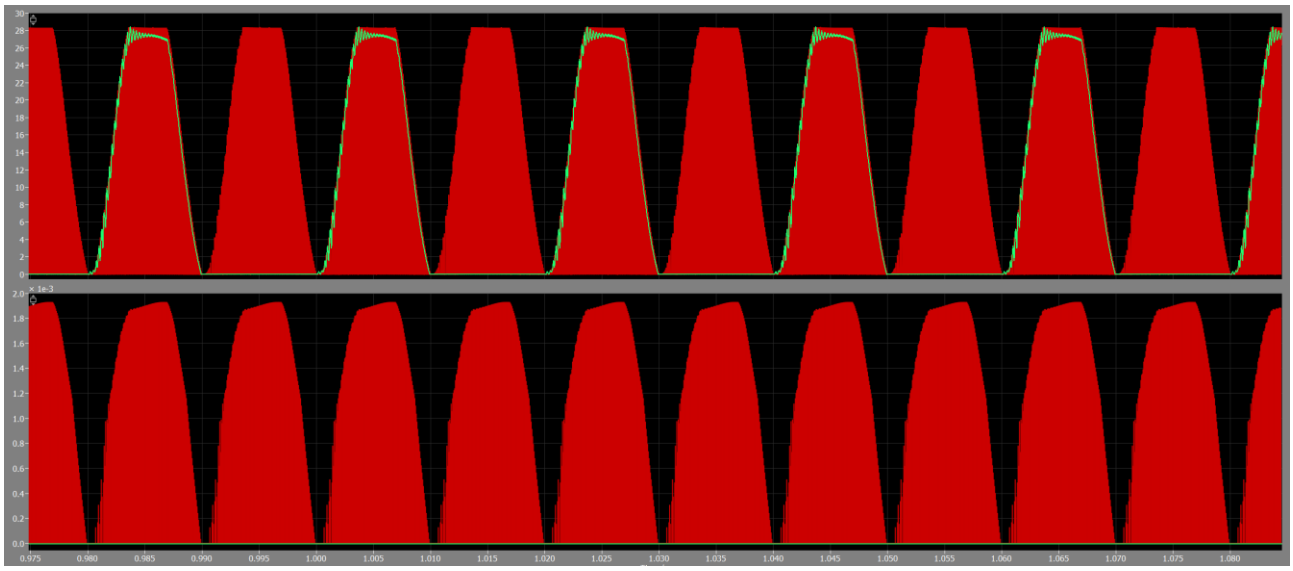


Vs



(Total -> -> IGBT conduction -> IGBT switching -> Diodes conduction -> Diode switching)

Diode losses



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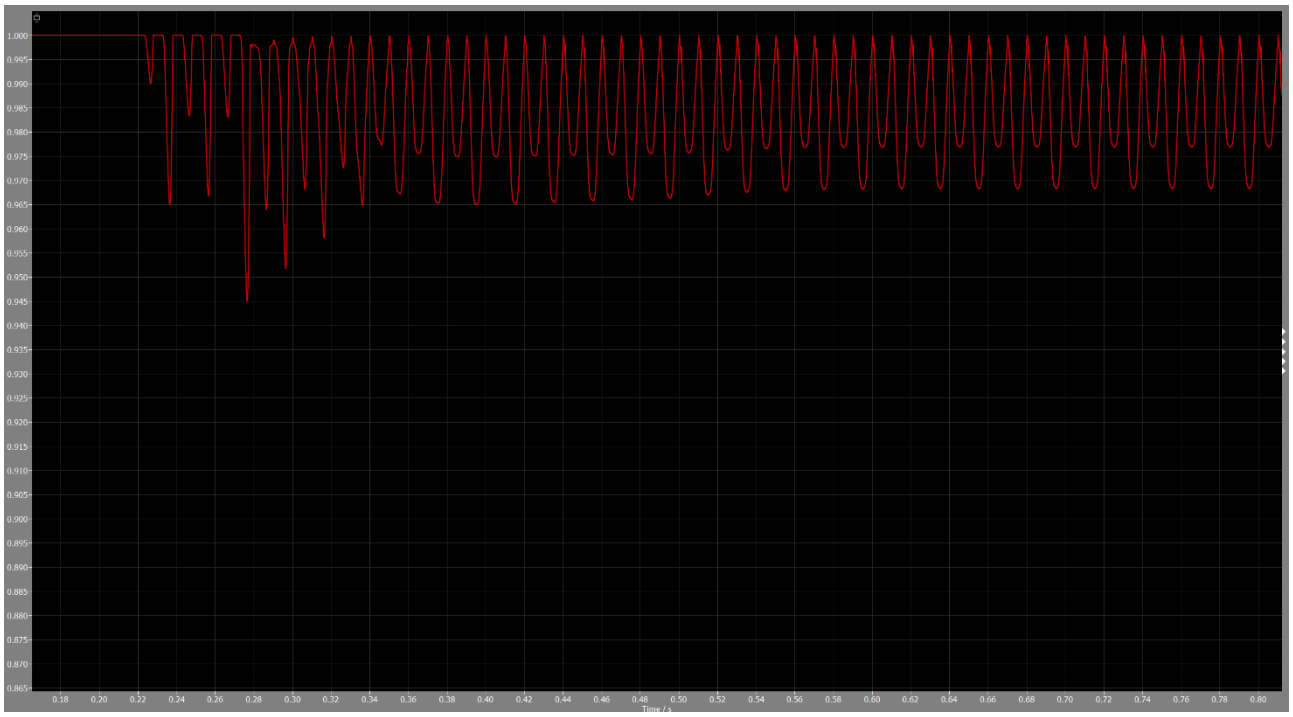
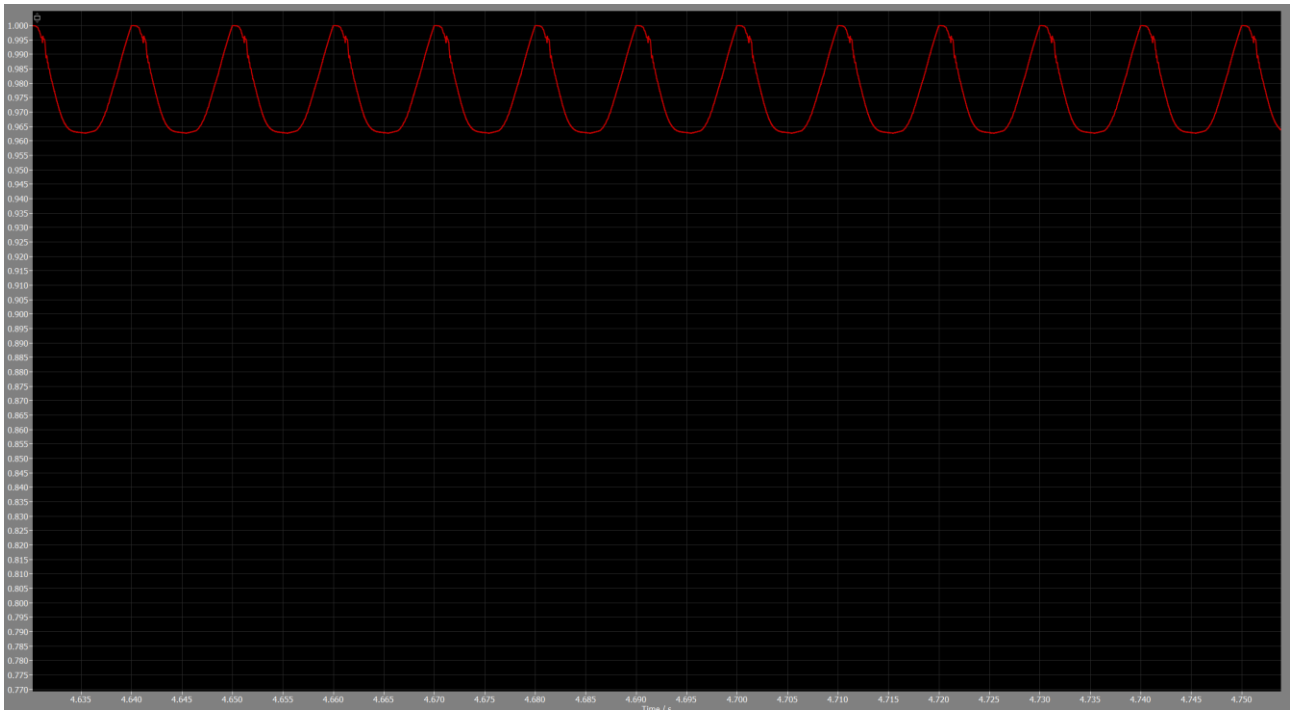
(Green : bridge; Red : boost)

For the diode: they all contribute for conduction losses but only the boost diode that operate at switching frequency is able to provide a distinguish switch current since in the bridge rectifier the phenomena is happen twice in a grid period.

Efficiency



Vs



(NB input power is the sum of the output power plus the thermal power)